4742 77603

SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

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Date 10/9/02 Serial # 10/015,757 Priority Application Date 12/22/00

Your Name M. Lewis Examiner #

AU 2822 Phone 305-3743 Room Plaza 3-3B00

In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

10-09-02 P03:41 IN

Where have you searched so far on this case?

Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other:

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements.

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other ___
Secondary Refs ✓ Foreign Patents ___
Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-11

Problem See Page 1 Lines 14-27
" 2 " 1-26

Solutions " " 2 " 1-19

Staff Use Only

Staff Use Only	Type of Search	Vendors
Searcher: Sode Fergu[illegible]	Structure (#)	STN
Searcher Phone: 703-605-1226	Bibliographic ✓	Dialog ✓
Searcher Location: STIC-EIC2800, CP4-9C18	Litigation	Questel/Orbit
Date Searcher Picked Up: 10-10-02	Fulltext ✓	Lexis-Nexis
Date Completed: 10-10-02	Patent Family	WWW/Internet
Searcher Prep/Rev Time: 45	Other	Other
Online Time: 240		

corrosion easily occurs. When a dummy fine line pattern is formed, so that an area ratio of the dummy fine line pattern to the entire wire patterns including a fine line pattern, a large pad pattern and the dummy fine line pattern, is larger than an area ratio of the fine line pattern to the entire wire patterns including the fine line pattern, the large pad pattern, and the dummy fine line pattern, the corrosion of the fine line pattern can be prevented.--

IN THE CLAIMS

Please amend claims 1, 3-5 and 7-11 to read as follows:

1. (Amended) A semiconductor device comprising:

a plurality of metal wire patterns which include a fine line pattern and pad patterns, an area of the fine line pattern being more than 1% of a total area of said plurality of metal wire patterns.

3. (Amended) The semiconductor device as recited in claim 1, wherein the pad patterns include connection pad patterns which electrically connect the pad patterns to the fine line pattern, said connection pad patterns being included in said total area.

4. (Amended) The semiconductor device as recited in claim 1, wherein the plurality of metal wire patterns are made of aluminum or copper.

5. (Amended) A semiconductor device comprising:

a plurality of metal wire patterns which include main fine line patterns, main pad patterns and dummy fine line patterns, an area of the dummy fine line patterns, which are connected to the pad patterns, being less than 1% of a total area of said plurality of metal wire patterns and also being less than a value obtained by dividing an area of the main fine line patterns by said total area.

7. (Amended) The semiconductor device as recited in claim 5, wherein the plurality of metal wire patterns are made of aluminum or copper wire.

8. (Amended) The semiconductor device as recited in claim 5, wherein the dummy fine line patterns do not form or contribute to any electric circuit.

9. (Amended) The semiconductor device as recited in claim 5, wherein the plurality of metal wire patterns further include dummy pad patterns, to which the dummy fine line patterns are connected, said dummy pad patterns and said dummy fine line patterns being electrically disconnected from the main fine line patterns and the main pad patterns.

10. (Amended) The semiconductor device as recited in claim 5, wherein the plurality of metal wire patterns further include dummy pad pool patterns, to which the dummy fine line

patterns are connected, said dummy pad pool patterns and said dummy fine line patterns being electrically disconnected from the main fine line patterns and the main pad patterns.

11. (Amended) The semiconductor device as recited in claim 5, wherein the plurality of metal wire patterns are made of aluminum or copper wire.

Please add the following claims:

--12. The semiconductor device as recited in claim 5, wherein the plurality of metal wire patterns further include connection pad patterns which electrically connect the main pad patterns to the fine line patterns, said connection pad patterns being included in said total area.

13. The semiconductor device as recited in claim 12, wherein the total area is represented by Ap+Ac+A+d, where, 'd' represents the area of the dummy fine line patterns, 'Ap' represents an area of the main pad patterns, 'Ac' represents an area of the connection pad patterns and 'A' represents the area of the main fine line patterns.--

SEMICONDUCTOR DEVICE CAPABLE OF PREVENTING CORROSION OF METAL WIRES FROM CMP (CHEMICAL MECHANICAL POLISHING) PROCESS

Field of the Invention

The present invention relates to a semiconductor device capable of preventing a corrosion of metal wires and, more particularly, to a semiconductor device capable of preventing a corrosion of metal wires from a chemical mechanical polishing (CMP) process.

Description of the Prior Art

Generally, wires of a semiconductor device have been formed by using a reactive ion etching (RIE) process. However, as the width of the wires becomes narrower, it is difficult to apply the RIE process to form wires so a damascene technology is introduced. In the damascene technology, a chemical polishing (CMP) process is necessary for an isolation of the wires. Accordingly, the CMP process for the Al or Cu wires is required. Al and Cu have lower hardness than tungsten (W), and also have a very high chemical activity, making the Al and Cu wires very susceptible to corrosion. Since the corrosion of the metal wires is fatal to the reliability of the semiconductor device, such corrosion has to be prevented.

The CMP process is a key process in forming wires when applying the damascene technology. Since the Al or Cu wire is

the electrically and chemically active metal, after the CMP process, a NH_4OH or HF solution, which is used at the conventional post cleaning process, cannot be used at a post cleaning process so that, if an appropriate chemical cleaner capable of being used at the post cleaning process is not developed, the post cleaning process is performed by using deionized (DI) water.

When the DI water is used as a post-process cleaner, a fine line, which is connected to a large pad, is more heavily corroded than an adjacent wide line. Since the corrosion is observed at a wafer cleaning process after the CMP process, another cleaning solution has to be used instead of the DI water. Recently, the wires are formed with copper and a low k insulating layer so that a research of the aluminum damascene process is weaker than the copper process. Accordingly, researches of CMP slurry and the post process cleaner are insufficiently developed.

The basic method for suppressing corrosion is to change a position, in which an oxidation reaction occurs. Namely, it is to use a material, which is electrically and chemically much more active than a material used as the wire, as a sacrificial anode. However, this requires a complicated process in which the sacrificial anode has to be formed at the same pattern with main wires. Also, it is not easy to select metals which are much more active material than aluminum or copper, which is usually used to form the wire.

Summary of the Invention

It is, therefore, an object of the present invention to provide a semiconductor device capable of preventing corrosion of metal wire patterns formed with aluminum or copper from the chemical-mechanical polishing (CMP) process.

In accordance with an aspect of the present invention, there is provided a semiconductor device comprising a plurality of metal wire patterns, each of which includes fine line patterns and pad patterns, wherein an area ratio of the fine line pattern to the entire wire patterns is above 1%.

In accordance with another aspect of the present invention, there is provided a semiconductor device comprising a plurality of metal wire patterns, each of which includes main fine line patterns, main pad patterns and dummy fine line patterns, wherein an area ratio of the dummy fine line patterns, which are connected to the pad patterns, to the entire wire patterns is below 1% and lower than that of the main fine line patterns.

Brief Description of the Drawings

The above and other objects and features of the instant invention will become apparent from the following description of preferred embodiments taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a schematic diagram showing a formation of metal wire patterns in accordance with a first embodiment of the present invention;

Fig. 2 is a schematic diagram showing a formation of metal wire patterns inserting dummy lines in accordance with a second embodiment of the present invention;

Fig. 3 is a schematic diagram showing a formation of metal wire patterns inserting dummy lines and large dummy pads in accordance with a third embodiment of the present invention; and

Fig. 4 is a schematic diagram showing a formation of metal wire patterns inserting dummy lines and large dummy pad pool in accordance with a fourth embodiment of the present invention.

Detailed Description of the Preferred Embodiments

Hereinafter, a method for preventing a corrosion of metal wire patterns formed with an aluminum or copper wire from the chemical-mechanical polishing (CMP) process will be described in detail referring to the accompanying drawings.

In order to basically prevent the corrosion of the metal wires formed with an Al or Cu wire according to the present invention, a dummy pattern, where corrosion can occur instead of a main wire pattern, is additionally inserted to a basic wire pattern. When a fine line pattern of sub-micron size is connected to a large pad pattern, the fine line pattern is easily corroded. This corrosion is a dependence of patterns

because the large pad pattern and the fine line pattern are formed with the same material. Particularly, when an area ratio of the fine line pattern to the overall wire patterns including the fine line pattern and the large pad pattern is low, the corrosion easily occurs so that, as a dummy fine line pattern, when an area ratio of the dummy fine line pattern to the entire wire patterns including a fine line pattern, a large pad pattern and the dummy fine line pattern, is larger than an area ratio of the narrow main line to the entire wires, is formed, the corrosion of the fine line pattern can be prevented.

Two method embodiments for preventing the wire corrosion will be described according to the present invention.

A first method is to differently form a pattern from the prior pattern. Namely, it is to change an area ratio of the fine line pattern to the entire wire patterns.

Fig. 1 is a schematic diagram showing the formation of metal wire patterns including a main fine line pattern 120, which has to be protected from corrosion, connected to large pad patterns 100 in accordance with a first embodiment of the present invention. After the CMP process of the wire patterns, the corrosion of the main fine line pattern 120 is caused when the main fine line pattern 120, when a width of the main fine line pattern is below 1 μm, is connected to the large pad patterns 100. When an area ratio of the main fine line pattern 120 to the entire wire patterns including the large pad patterns 100, connection pad pattern 110 and the main fine line pattern

120 is approximately above 1%, the corrosion can be prevented. A formula for preventing the corrosion is as follows:

$$(A/(Ap+Ac+A)) \times 100) > 1\%$$

where, 'A' represents an area of the main fine line pattern 120, 'Ap' represents a gross area of the large pad patterns 100 and 'Ac' represents a gross area of the connection pad patterns 110.

A second method for preventing the corrosion of the main fine line pattern is to additionally insert a dummy fine line pattern to the basic wire patterns.

Fig. 2 is a schematic diagram showing a formation of metal wire patterns using dummy fine line patterns 220 connected to the large pad patterns 200 for preventing a corrosion of the main fine line pattern 230 in accordance with a second embodiment of the present invention.

Referring to Fig. 2, the dummy fine line patterns 220 are connected to the large pad patterns 200 and formed parallel with the main fine line pattern 230, which is desired to prevent the corrosion. When an area ratio of the dummy fine line patterns 220 to the entire wire patterns is much lower than an area ratio of the main fine line pattern 230 to the entire wire patterns and is below 1%, the corrosion of the main fine line pattern 230 can be prevented. A formula for preventing the corrosion according to this second embodiment is as follows:

$$(d/(Ap+Ac+A+d) \times 100) < 1\% \text{ and,}$$

$$d/(Ap+Ac+A+d) < A/(Ap+Ac+A+d)$$

where, 'd' represents a gross area of the dummy fine line patterns 220, 'Ap' represents a gross area of the large pad patterns 200, 'Ac' represents a gross area of the connection pad patterns 210 and 'A' represents an area of the main fine line pattern 230. Also, the dummy fine line patterns 220 do not make any electric circuit.

Fig. 3 is a schematic diagram showing a formation of metal wire patterns using dummy fine line patterns 340 connected to large dummy pad patterns 330 for preventing the corrosion of a main fine line pattern 320 in accordance with a third embodiment of the present invention of the present invention. The large dummy pad patterns 330 and the dummy fine line patterns 340 do not make any electric circuit.

A formula for preventing the corrosion of the main fine line pattern 320 is as follows:

$(d/(D+d)) \times 100 < 1\%$ and,

$(d/(D+d)) < A/(Ap+Ac+A)$

where, 'd' represents a gross area of the dummy fine line patterns 340 and 'D' represents an gross area of the large dummy pad patterns 330. Also, 'A' represents an area of the main fine line pattern 320, 'Ap' represents a gross area of the large pad patterns 300 and 'Ac' represents a gross area of connection pad patterns 310. At this time, the large dummy pad patterns 330 and the dummy fine line patterns 340 are electrically disconnected from the main wire patterns.

Fig. 4 is a schematic diagram showing a formation of metal wire patterns using a dummy pad pool 440 and dummy fine line patterns 430A and 430B to be used in several modules for the same purpose of preventing corrosion of the main fine line patterns 420A and 420B in accordance with a fourth embodiment of the present invention.

Referring to Fig. 4, in order to prevent the corrosion of the main fine line pattern 420A in an 'X' part, a formula for area ratios is as follows:

$(d1/(D+d1+d2)\ X\ 100) < 1\%$ and,

$(d1/(D+d1+d2) < A1/(A1p+A1c+A1)$

where, 'd1' represents a gross area of the dummy line patterns 430A, 'd2' represents a gross area of the dummy line patterns 430B, 'D' represents an area of the dummy pad pool 440. Also, 'A1' represents an area of the main fine line pattern 420A, 'A1p' represents a gross area of the large pad pattern 400A and 'A1c' represents a gross area of connection pad patterns 410A.

Also, in order to prevent the corrosion of the main fine line pattern 420B in a 'Y' part, a formula for area ratios in as follows:

$(d2/(D+d1+d2)\ X\ 100 < 1\%$ and,

$(d2/(D+d1+d2) < A2/(A2p+A2c+A2)$

where, 'd2' represents a gross area of the dummy line patterns 430B, 'd1' represents a gross area of the dummy line patterns 430A, 'D' represents an area of the dummy pad pool 440.

Also, 'A2' represents an area of the main fine line pattern 420B, 'A2p' represents a gross area of the large pad pattern 400B and 'A2c' represents a gross area of connection pad patterns 410B. The dummy pad pool 440 and the dummy fine line patterns 430A and 430B do not make any electric circuit.

Accordingly, the present invention can be applied in the damascene technology even if slurries for polishing metal wire patterns, such as Al or Cu wires, and cleaners, which are appropriate at a post cleaning process, are not developed.

While the present invention has been described with respect to the particular embodiments, it will be apparent to those skilled in the art that various changes and modifications may be made without departing from the spirit and scope of the invention as defined in the following claims.

What is claimed is:

1. A semiconductor device comprising:

a plurality of metal wire patterns, each of which includes a fine line pattern and pad patterns, wherein an area ratio of the fine line pattern to an overall wire pattern is greater than 1%.

2. The semiconductor device as recited in claim 1, wherein a width of the fine line pattern is below sub-micron.

3. The semiconductor device as recited in claim 1, wherein the pad patterns include connection pad patterns which electrically connect the pad patterns to the fine line pattern, said connection pad patterns being included in said overall wire pattern.

4. The semiconductor device as recited in claim 1, wherein the metal wire patterns are made of aluminum or copper.

5. A semiconductor device comprising:

a plurality of metal wire patterns, each of which includes main fine line patterns, main pad patterns and dummy fine line patterns, wherein an area ratio of the dummy fine line patterns, which are connected to the pad patterns, to an entire wire

pattern is less than 1% and lower than that of an area ratio of the main fine line patterns to the entire wire pattern.

6. The semiconductor device as recited in claim 5, wherein the dummy fine line patterns are formed parallel with the main fine line patterns at a distance of a width of the main fine line pattern.

7. The semiconductor device as recited in claim 5, wherein the metal wire patterns are made of aluminum or copper wire.

8. The semiconductor device as recited in claim 5, wherein the dummy fine line patterns do not make any electric circuit.

9. The semiconductor device as recited in claim 5, wherein the metal wire patterns further include dummy pad patterns, to which the dummy fine line patterns are connected, wherein the dummy pad patterns and the dummy fine line patterns are electrically disconnected from the main fine line patterns and the main pad patterns.

10. The semiconductor device as recited in claim 5, wherein the metal wire patterns further include dummy pad pool patterns, to which the dummy fine line patterns are connected, wherein the dummy pad pool patterns and the dummy fine line patterns are

electrically disconnected from the main fine line patterns and the main pad patterns.

11. The semiconductor device as recited in claim 5, wherein the metal wire patterns are made of aluminum or copper wire.

Abstract of the Disclosure

A semiconductor device comprising a plurality of metal wire patterns, each of which includes main fine line patterns, main pad patterns and dummy fine line patterns, wherein an area ratio of the dummy fine line patterns, which are connected to the main pad patterns, to the entire wire patterns is less than 1% and lower than a ratio of the main fine line patterns to the entire wire patterns.

FIG. 1

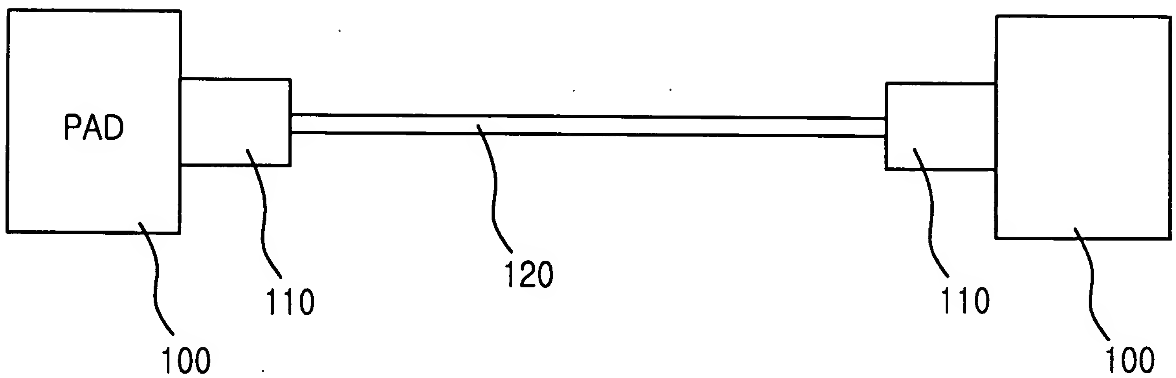


FIG. 2

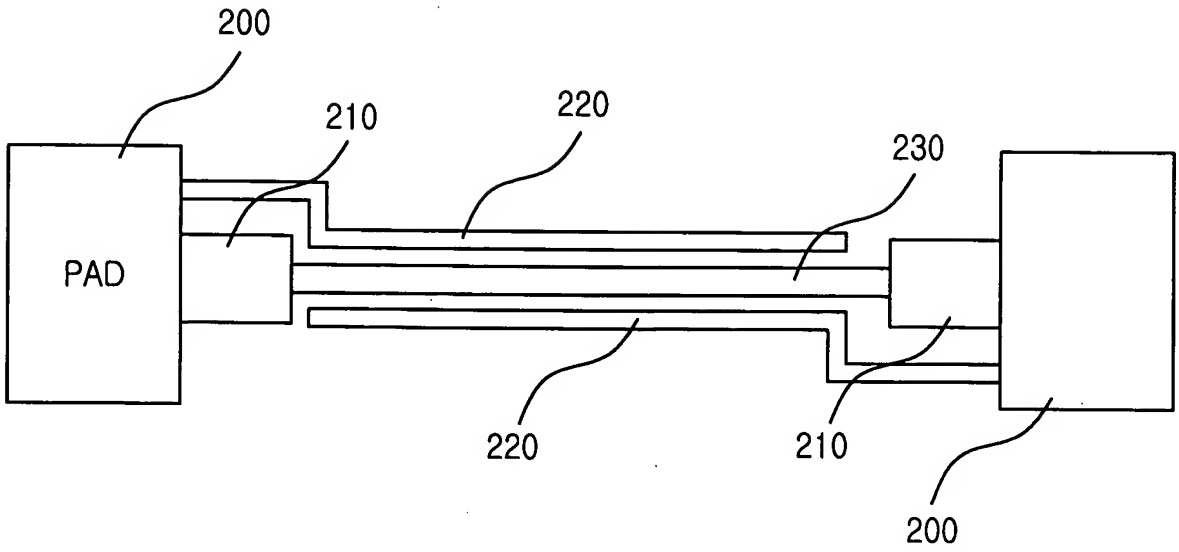

200
210
220
230
PAD
220
210
200

FIG. 3

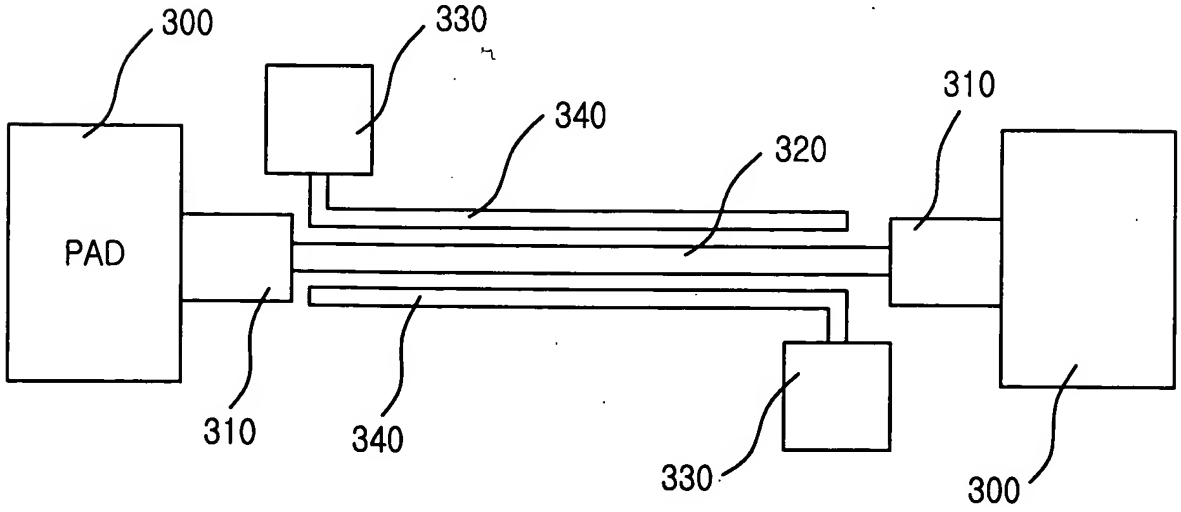
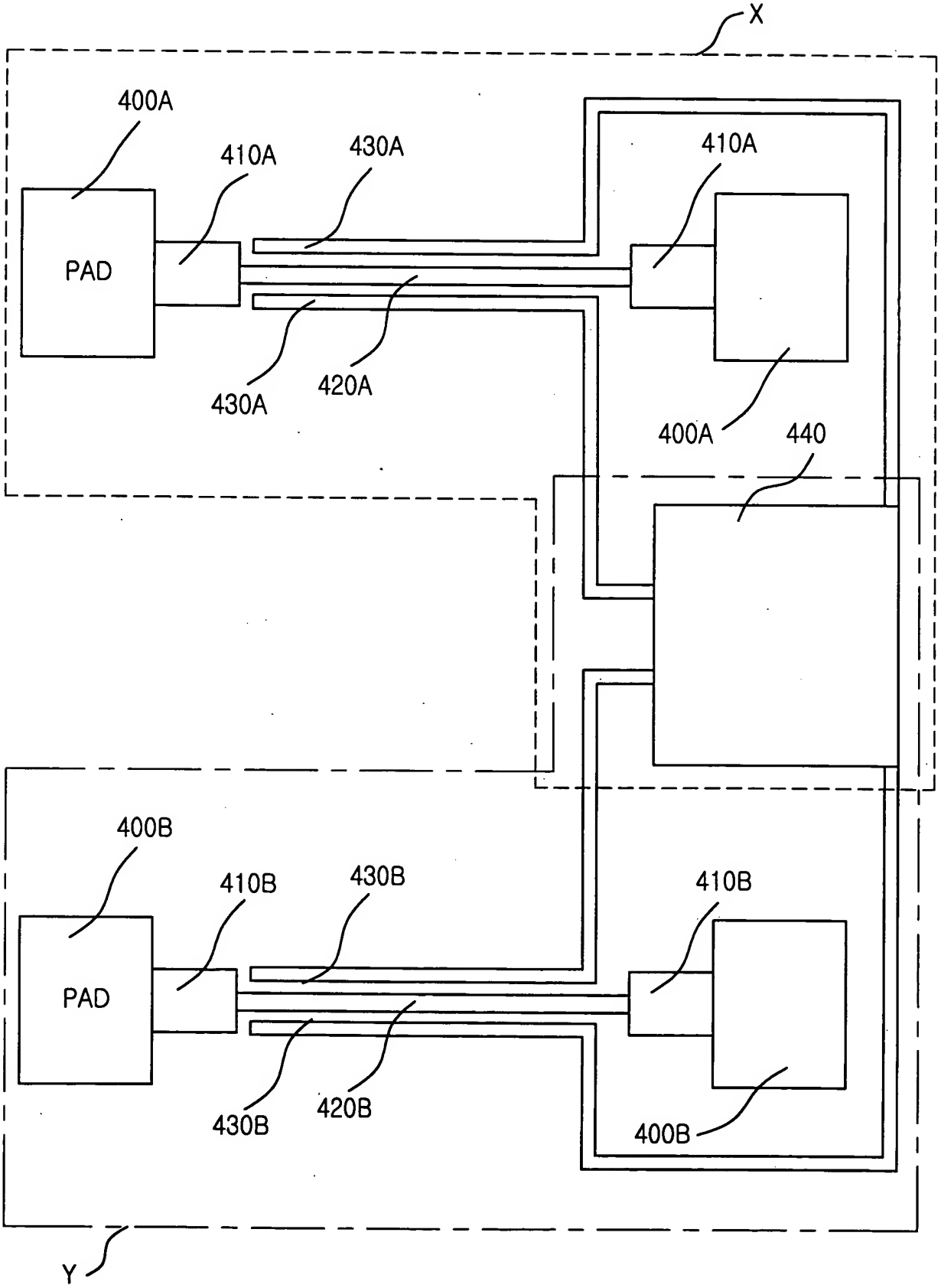

300
330
340
310
320
PAD
310
340
330
300

FIG. 4


X
400A
410A
430A
410A
PAD
430A
420A
400A
440
400B
410B
430B
410B
PAD
430B
420B
400B
Y

To: Monica Lewis
From: Bode Fagbohunka
Subject: Online Search
Date:- March 31, 2003

Please find attached the results of your search for 10015757. The search was conducted using the standard collection of databases on dialog for EIC 2800. The tagged references appear to be the closest references located during our search.

If you would like a re-focus please let me know or if you have any questions regarding the search results please do not hesitate to contact me.

Bode Fagbohunka
703-605-1726

```
Set     Items   Description
S1   10829420   PREVENT? OR AVOID? OR PRECLUD? OR PROHIBIT? OR REDUC? OR E-
             LIMINAT?
S2    2126896   CORROSION? OR DECAY? OR RUST? OR DETERIORAT? OR DECOMPOS? -
             OR OXIDI?AT?
S3     238587   CMP OR CHEMICAL()MECHANICAL()(POLISH? OR PLANAR?) OR POLIS-
             H? OR PLANARI?
S4       3572   (MAIN OR CONNECT?)()(PAD OR PADS)
S5    3379163   METAL()WIRE? OR AL OR CU OR ALUMINUM OR COPPER
S6       8031   (DUMMY OR FINE)()LIN???
S7    2759251   RATIO? ?
S8       4253   S1 AND S2 AND S3
S9        795   S1(10N)S2(10N)S3
S10         0   S9 AND S4  AND S5 AND S6 AND S7
S11         0   S9 AND S4  AND S5 AND S6
S12         2   S9 AND S6 AND (S4 OR S5)
S13         2   RD (unique items)
S14      5312   MAIN(2N)(PADS OR PAD OR PATTERN?)
S15         0   S9 AND S14 AND S6
S16       520   S1(6N)S2(6N)S3
S17         0   S16 AND S6
S18         2   S16 AND DUMMY
S19         2   S18 NOT S13
S20         6   S9 AND DUMMY
S21         2   S20 NOT (S18 OR S13)
S22      1451   S8 AND S5
S23         2   S22 AND (S6 OR S14)
S24         4   S22 AND LINE?()PATTERN?
S25         6   S22 AND LINE?(3N)PATTERN?
S26         0   S25 AND RATIO
S27         0   S25 NOT (S22 OR S20 OR S18 OR S13)
?  show files
File 315:ChemEng & Biotec Abs 1970-2003/Mar
         (c) 2003 DECHEMA
File   2:INSPEC 1969-2003/Mar W4
         (c) 2003 Institution of Electrical Engineers
File   6:NTIS 1964-2003/Mar W5
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File 144:Pascal 1973-2003/Mar W4
         (c) 2003 INIST/CNRS
File  99:Wilson Appl. Sci & Tech Abs 1983-2003/Feb
         (c) 2003 The HW Wilson Co.
File  94:JICST-EPlus 1985-2003/Mar W5
         (c)2003 Japan Science and Tech Corp(JST)
File  35:Dissertation Abs Online 1861-2003/Mar
         (c) 2003 ProQuest Info&Learning
File  65:Inside Conferences 1993-2003/Mar W5
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File 347:JAPIO Oct 1976-2002/Nov(Updated 030306)
         (c) 2003 JPO & JAPIO
File 350:Derwent WPIX 1963-2003/UD,UM &UP=200321
         (c) 2003  Thomson Derwent
?
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13/9/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7386675 INSPEC Abstract Number: B2002-10-2550E-128
Title: Control of pattern specific corrosion during aluminum **chemical mechanical polishing**
Author(s): Hyungjun Kim; Panki Kwon; Sukjae Lee; Hyung-hwan Kim; Sang-ick Lee; Seo-young Song; Chul-woo Nam
Author Affiliation: Memory R&D Div., Hynix Semicond. Inc, Ichon, South Korea
Conference Title: Chemical-Mechanical Polishing 2001 - Advances and Future Challenges. Symposium (Materials Research Society Symposium Proceedings Vol.671) p.M6.5.1-6
Editor(s): Babu, S.V.; Cadien, K.C.; Yano, H.
Publisher: Mater. Res. Soc, Warrendale, PA, USA
Publication Date: 2001 Country of Publication: USA xi+288 pp.
ISBN: 1 55899 607 9 Material Identity Number: XX-2002-01118
Conference Title: Chemical-Mechanical Polishing 2001 - Advances and Future Challenges. Symposium
Conference Date: 18-20 April 2000 Conference Location: San Francisco, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Experimental (X)
Abstract: A pattern specific **corrosion** of **aluminum** wires was found during **aluminum chemical mechanical polishing** process. This paper presents and discusses the particular pattern dependency of the **corrosion** behavior and effective control methods in order to **reduce** the corrosion. An **aluminum** single damascene structure on silicon dioxide thin film was prepared and the effects of process variables and pattern configuration on corrosion behavior were extensively explored. The corrosion behavior was quantitatively analyzed using sheet resistance of the corroded line. It was demonstrated that corrosion of **aluminum** wire was associated with cleaning media and pattern configuration. The area ratio between sub-micron size line and pads was the most important factors to determine the corrosion behavior. A post cleaning chemical including corrosion inhibitor could not prevent the corrosion perfectly. It was found that sacrificial **dummy lines** could reduce the **aluminum** corrosion, which suggests that the **aluminum** corrosion could be controlled by the structural consideration in **aluminum** damascene. (3 Refs)
Subfile: B
Descriptors: aluminium; chemical mechanical polishing; corrosion resistance; integrated circuit interconnections; integrated circuit metallisation
Identifiers: pattern specific corrosion control; chemical mechanical polishing process; **Al** CMP process; corrosion behavior; **Al** single damascene structure; process variables; pattern configuration; sheet resistance; area ratio effect; line width effect; cleaning media; submicron size line; submicron size pads; sacrificial **dummy lines** ; **Al** corrosion ; corrosion inhibitor; corrosion resistance; deionized water; **Al** -SiO/sub 2/
Class Codes: B2550E (Surface treatment (semiconductor technology)); B2550F (Metallisation and interconnection technology)
Chemical Indexing:
Al-SiO2 int - SiO2 int - Al int - O2 int - Si int - O int - SiO2 bin - O2 bin - Si bin - O bin - Al el (Elements - 1,2,3)

13/9/2 (Item 1 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)

06084393 E.I. No: EIP02277005058
Title: Control of pattern specific corrosion during aluminum **chemical mechanical polishing**
Author: Kim, Hyungjun; Kwon, Panki; Lee, Sukjae; Kim, Hyung-Hwan; Lee, Sang-Ick; Song, Seo-Young; Nam, Chul-Woo
Corporate Source: Memory R and D Division Hynix Semiconductor Inc., Ichon, South Korea
Conference Title: Chemical - Mechanical Polishing 2001 - Advances and Future Challenges
Conference Location: San Francisco, CA, United States Conference Date: 20010418-20010420
E.I. Conference No.: 59211
Source: Materials Research Society Symposium - Proceedings v 671 2001. p M6.5.1-M6.5.6
Publication Year: 2001
CODEN: MRSPDH ISSN: 0272-9172
Language: English
Document Type: CA; (Conference Article) Treatment: X; (Experimental)
Journal Announcement: 0207W2
Abstract: A pattern specific **corrosion** of **aluminum** wires was found during **aluminum chemical mechanical polishing** process. This paper presents and discusses the particular pattern dependency of the **corrosion** behavior and effective control methods in order to **reduce** the corrosion. An **aluminum** single damascene structure on silicon dioxide thin film was prepared and the effects of process variables and pattern configuration on corrosion behavior were extensively explored. The corrosion behavior was quantitatively analyzed using sheet resistance of corroded line. It was demonstrated that corrosion of **aluminum**0 wire was associated with cleaning media and pattern configuration. The area ratio between sub-micron size line and pads was the most important factors to determine the corrosion behavior. A post cleaning chemical including corrosion inhibitor couldn't prevent the corrosion perfectly. It was found that sacrificial **dummy lines** could reduce the **aluminum** corrosion, which suggests that the **aluminum** corrosion could be controlled by the structural consideration in **aluminum** damascene. 3 Refs.
Descriptors: Chemical mechanical polishing; Corrosion; **Aluminum** ; Wire; Silica; Association reactions; Cleaning; Corrosion inhibitors; Numerical analysis
Identifiers: **Aluminum** wires; Pattern specific corrosion
Classification Codes:
802.3 (Chemical Operations); 539.1 (Metals Corrosion); 541.1 (Aluminum); 535.2 (Metal Forming); 804.2 (Inorganic Compounds); 802.2 (Chemical Reactions)
802 (Chemical Apparatus & Plants; Unit Operations; Unit Processes); 539 (Metals Corrosion & Protection; Metal Plating); 541 (Aluminum & Alloys); 535 (Rolling, Forging & Forming); 804 (Chemical Products Generally)
80 (CHEMICAL ENGINEERING, GENERAL); 53 (METALLURGICAL ENGINEERING, GENERAL); 54 (METALLURGICAL ENGINEERING, METAL GROUPS)
?

19/9/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06622581 **Image available**
ALIGNMENT MARK STRUCTURE HAVING PROTECTIVE **DUMMY** PATTERN FOR PRODUCTION OF SEMICONDUCTOR

PUB. NO.: 2000-208392 [JP 2000208392 A]
PUBLISHED: July 28, 2000 (20000728)
INVENTOR(s): CHIN KACHEN
APPLICANT(s): UNITED MICROELECTRONICS CORP
APPL. NO.: 11-004863 [JP 994863]
FILED: January 12, 1999 (19990112)
INTL CLASS: H01L-021/027; G03F-001/08

ABSTRACT

PROBLEM TO BE SOLVED: To provide an alignment mark structure in which an alignment mark on a wafer is not damaged or deteriorated through CMP process but definite quality of the alignment mark can be sustained visually.

SOLUTION: An alignment mark structure having a protective **dummy** pattern for production of semiconductor is provided wherein the alignment mark on a wafer is protected such that the mark is not damaged definite quality is not deteriorated visually by chemical mechanical polishing(CMP). The alignment mark structure has a scribe line of wafer or an alignment mark 102 formed in the region of a nonconstitutional part, and a protective **dummy** pattern 114 for protecting it against CMP. The protective **dummy** pattern 114 has uniform density substantially equal to that of the constitutional part region of the wafer. Since the alignment mark structure protects the alignment mark against damage and **prevents** the alignment mark from being **deteriorated** through **CMP** process, definite quality of the alignment mark 102 can be sustained visually.

19/9/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014082984 **Image available**
WPI Acc No: 2001-567198/200164
XRPX Acc No: N01-422383
Dummy **pattern for high density arrays, has metal wiring parallel to wirings within high density array**
Patent Assignee: LIANHUA ELECTRONICS CO LTD (LIAN-N)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001007107	A	20010112	JP 99165424	A	19990611	200164	B

Priority Applications (No Type Date): JP 99165424 A 19990611
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001007107	A		6	H01L-021/3205	

Abstract (Basic): JP 2001007107 A

NOVELTY - **Dummy** pattern (210) consists of metal wiring (216) arranged in parallel to wirings (214a,214b) in the high density array (206). The width of metal wiring is similar to that of parallel wirings.

USE - For preventing generation of excessive corrosion in high density arrays, during dual damascene process.

ADVANTAGE - **Dummy** pattern **prevents** generation of excessive **corrosion** within the high density array during chemo-mechanical **polishing** .

DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of the **dummy** pattern for preventing generation of excessive corrosion within the high density array.

High density array (206)

Dummy pattern (210)

Wirings (214a,214b)

Metal wiring (216)

pp; 6 DwgNo 2/5

Title Terms: **DUMMY** ; PATTERN; HIGH; DENSITY; ARRAY; METAL; WIRE; PARALLEL; WIRE; HIGH; DENSITY; ARRAY

Derwent Class: U11

International Patent Class (Main): H01L-021/3205

File Segment: EPI

Manual Codes (EPI/S-X): U11-D01A6

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21/9/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

07056718 **Image available**
METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

PUB. NO.: 2001-284354 [JP 2001284354 A]
PUBLISHED: October 12, 2001 (20011012)
INVENTOR(s): KAMIKUBO NORITAKA
APPLICANT(s): SHARP CORP
APPL. NO.: 2000-092732 [JP 200092732]
FILED: March 30, 2000 (20000330)
INTL CLASS: H01L-021/3205; H01L-021/768

ABSTRACT

PROBLEM TO BE SOLVED: To solve the problem, where because of the polishing rate difference, some regions were polished excessively, to **reduce** the thickness of a layer insulation film, resulting in the nonconformity that the **planarity** of the layer insulation film is **deteriorated** , after forming through-hole plugs.

SOLUTION: The semiconductor device manufacturing method comprises a step of forming connection hole forming openings 6 and **dummy** hole forming openings 7, each having a less opening area than that of the opening 6 on a second layer insulation film 4, forming a resist pattern 5 thereon, so that the area of a maximum region where the openings 6, 7 are not formed, is less than that of a region of 100 μm in radius, etching the second layer insulation film 4, using the resist pattern 5 as an etching mask, simultaneously forming connection holes 6a and **dummy** holes 7a, depositing a plug material so as to fill the connecting holes and the **dummy** holes, and chemical-mechanical polishing to form connection plugs and **dummy** plugs.

21/9/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

06179861 **Image available**
METHOD AND DEVICE FOR POLISHING SEMICONDUCTOR DEVICE

PUB. NO.: 11-121410 [JP 11121410 A]
PUBLISHED: April 30, 1999 (19990430)
INVENTOR(s): SHINADA KUNINORI
KASAI TOSHIO
APPLICANT(s): NIKON CORP
APPL. NO.: 09-293155 [JP 97293155]
FILED: October 13, 1997 (19971013)
INTL CLASS: H01L-021/304; B24B-037/04

ABSTRACT

PROBLEM TO BE SOLVED: To **eliminate** occurrence of shape degradation or work **decomposition** layer of a semiconductor device.

SOLUTION: A **dummy** ring 14 is pressed against a **polisher** 4 by an air cylinder of a coarse movement Z table. A semiconductor device 26 is so

pressed by an air cylinder 22 as to be positioned on the same polisher surface before starting polishing, and under the state, the air cylinder 22 is air-locked to fix an upper and lower positions of the semiconductor device 26. During polishing process, only the semiconductor device 26 is polished while the **dummy** ring 14 polished little. As the polishing progresses, the semiconductor device 26 contacting to the polisher at first gradually shifts to non-contact state. At the non-contact polishing, an unevenness at a top surface layer part of the semiconductor device 26 which occurred at contact-state polishing is removed by etching.

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Set      Items   Description
S1     2854185   PREVENT? OR AVOID? OR PRECLUD? OR PROHIBIT? OR REDUC? OR E-
             LIMINAT?
S2      331915   CORROSION? OR DECAY? OR RUST? OR DETERIORAT? OR DECOMPOS? -
             OR OXIDI?AT?
S3      247904   CMP OR CHEMICAL()MECHANICAL()(POLISH? OR PLANAR?) OR POLIS-
             H? OR PLANARI?
S4       61640   (METAL OR AL OR CU OR ALUMINUM OR COPPER)(3N)WIRE?
S5       36494   (DUMMY OR DUMMIES OR FINE OR MAIN)(3N)(LINE OR LINES OR PA-
             TTERN?)
S6           0   S1(S)S2(S)S3(S)S4(S)S5
S7          13   S1(S)S2(S)S3(S)(S4 OR S5)
? show files
File 349:PCT FULLTEXT 1979-2002/UB=20030327,UT=20030320
         (c) 2003 WIPO/Univentio
File 348:EUROPEAN PATENTS 1978-2003/Mar W03
         (c) 2003 European Patent Office
File  16:Gale Group PROMT(R) 1990-2003/Mar 31
         (c) 2003 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
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7/TI,PN,PD,AN,AD,AB,K/4 (Item 4 from file: 349)

CU-PAD/BONDED/CU-WIRE WITH SELF-PASSIVATING CU-ALLOYS
FIL DE CUIVRE SOUDE A UNE PASTILLE DE CUIVRE AVEC DES ALLIAGES DE CUIVRE D'AUTO-PASSIVATION

Patent and Priority Information (Country, Number, Date):
Patent: WO 200254491 A2 20020711 (WO 0254491)
Application: WO 2001US43960 20011114 (PCT/WO US0143960)

English Abstract
In an integrated circuit structure, the improvement comprising a wire bonded Cu-pad with Cu-wire component, wherein the Cu-pad Cu-wire component is characterized by self-passivation, low resistance, high bond strength, and improved resistance to oxidation and corrosion, the Cu-pad Cu-wire component comprising: a metallization-line; a liner separating the metallization line and a Cu-alloysurrounding a Cu-pad; a dielectric surrounding the liner; anda Cu-pad bonded to a Cu-alloy wire; the Cu-wire component being characterized by self-passivation areas on: a) a dopant rich interface in between the Cu-alloy and liner; b) a surface of the Cu-pad; c) a surface of the bond between the Cu-pad and the Cu-alloy wire; and d) a surface of the Cu-alloy wire.

French Abstract
Dans un structure de circuit integre, l'amelioration concerne une pastille de cuivre (Cu) a soudure de fil avec une composante de fil de cuivre (Cu), cette composante de fil de Cu de pastille de Cu etant caracterisee par l'auto-passivation, une faible resistance, une grande force de soudure, et une resistance amelioree a l'oxydation et a la corrosion. Cette composante de fil de Cu de pastille de Cu comprend: une ligne de metallisation, un separateur separant la ligne de metallisation et un alliage de Cu entourant une pastille de Cu, un dielectrique entourant le separateur, et une pastille de Cu soudee a un fil d'alliage de Cu, cette composante de fil de Cu etant caracterisee par des zones d'auto-passivation sur: a) une interface riche en dopant situee entre l'alliage de Cu et le separateur, b) une surface de la pastille de Cu, c) une surface de la soudure entre la pastille de Cu et le fil d'alliage de Cu, et d) une surface du fil d'alliage de Cu.

Fulltext Availability:
Claims

Claim
... layer for final Cu-fill;
d) filling said damascene structure with pure Cu;
e) pre- **CMP** annealing at low temperatures (<2000C), to form a low resistive Cu film with large Cu grains;
and **prevent** out-diffusion of dopants in the Cu-alloy;
f) Cu- **CMP** to remove Cu-overfill, and by liner **CMP** ;
g) post **CMP** annealing at a temperature range of from about 2500C to about 4500C to form a...

...surface for probing;
j) probing the chips;
k) wirebonding of the probed pads with the **Cu** -alloy **wires** ;
and
1) annealing the bonded chips at temperatures between about 250C to about 4500C to form a self
10

passivating layer on the open Cu-pad surface and on the **Cu - wire** .

9 The process of claim 8 wherein, after step a), step b) is eliminated by...

...layer for final Cu-fill;
d) filling said damascene structure with pure Cu;
e) pre- **CMP** annealing at low temperatures (<2000C), to form a low resistive Cu film with large Cu grains; and **prevent** out-diffusion of dopants in the Cu alloy;
f) Cu- **CMP** to remove Cu-overfill, and by liner **CMP** ;
g) depositing a dielectric cap layer;
h) annealing at a temperature of from about 2500C...

...surface for probing;
k) probing the chips;
1) wirebonding of the probed pads with the **Cu** -alloy **wires** ; and
M) annealing the bonded chips at temperatures between about 2500C to about 4500C to form a self-passivating layer on the open Cu-pad surface and on the **Cu - Wire** .

11 The process of claim 10 wherein, after step a); step b) is eliminated by...

...layer for final Cu-fill;
d) filling said damascene structure with pure Cu;
e) pre- **CMP** annealing at low temperatures (<2000C), to form a low resistive Cu film with large Cu grains; and **prevent** out-diffusion of dopants in the Cu alloy;
f) Cu- **CMP** to remove Cu-overfill, and by liner **CMP** ;
g) post **CMP** annealing at a temperature of from about 2500C to about 4000C to form a partially...surface for probing;
12
) probing the chips;
M) wirebonding of the probed pads with the **Cu** -alloy **wires** ; and
n) annealing the bonded chips at temperatures between 2 5 00 C to about...

...to form a self-passivating layer on the open Cu-pad surface and on the **Cu - Wire** .

13 The process of claim 12 wherein, after step a); step b) is eliminated by...

...layer for final Cu-fill;
d) filling said damascene structure with pure Cu;
e) pre- **CMP** annealing at low temperatures (<2000C), to form a low resistive Cu film with large Cu grains; and **prevent** out-diffusion of dopants in the Cu-alloy;
f) cu- **CMP** to remove Cu-overfill, and by liner **CMP** ;
g) post **CMP** annealing at a temperature range of from about 2500C to about 4500C to form a...

...surface for
probing;
k) probing the chips;
13
) wirebonding of the probed pads with the Cu -alloy
wires ; and
m) annealing the bonded chips at temperatures between
about 2500C to about 4500C to form a self-passivating
layer on the open Cu-pad surface and on the **Cu - wire** .

15 The process of claim 15 wherein, between after step
a), step b) is eliminated...
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